Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec– 2018**

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| **Code :** | **17EC3048** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ANALOG VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course Outcome** | **Marks** |
| 1. | a. | Describe the dc BJT model with the explanation of all regions of operation. | CO2 | 15 |
| b. | Justify the necessity of dc and small signal models in device modeling. | CO2 | 5 |
| (OR) | | | |  |
| 2. | a. | Discuss the high frequency BJT Model in detail. | CO2 | 16 |
| b. | Illustrate the need for learning high frequency model. | CO2 | 4 |
|  |  |  |  |  |
| 3. | a. | Explain Successive approximation ADC in detail. | CO3 | 10 |
| b. | Discuss the voltage scaling D/A Converters. | CO3 | 10 |
| (OR) | | | |  |
| 4. | a. | Explain Parallel ADC in detail. | CO3 | 10 |
| b. | Discuss the Charge scaling D/A Converters. | CO3 | 10 |
|  |  |  |  |  |
| 5. | a. | Design a Parallel switched capacitor resistor emulation. | CO3 | 14 |
| b. | Give an overview on Switched capacitor amplifier. | CO3 | 6 |
| (OR) | | | |  |
| 6. | a. | Design a series parallel capacitor resistor emulation. | CO3 | 14 |
| b. | Give an overview on Switched capacitor Integrator. | CO3 | 6 |
|  |  |  |  |  |
| 7. | a. | Design a CMOS Differential amplifier using current mirror as load. | CO6 | 14 |
|  | b. | Give an overview of Current sink and Active load inverters. | CO6 | 6 |
| (OR) | | | |  |
| 8. | a. | Design a cascade amplifier with current mirror as load. | CO6 | 10 |
| b. | Design a CMOS differential amplifier using p channel MOSFET. | CO6 | 10 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | Give an overview on class A amplifiers and design a simple class A output stage. | CO6 | 10 |
| b. | Design a two stage open loop comparator. | CO6 | 10 |